This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11 (Canceled)

12. (Currently Amended) An image processing apparatus comprising:

a first element array having a plurality of photoelectric conversion elements arranged in a line;

a second element array shifted from said first element array by a predetermined distance in a main scanning direction and having a plurality of photoelectric conversion elements arranged in a line;

a first CCD shift register for serially transferring signals from said first element array in response to transfer pulses;

a second CCD shift register for serially transferring signals from said second element array in response to the transfer pulses; and

a pulse supply unit for supplying three types of the transfer pulses having different phases to said first CCD shift register and supplying three types of the transfer pulses having different pulses to said second CCD shift register;

wherein said pulse supply unit supplies, in a low-resolution mode, said three types of the transfer pulses having different phases to said first and second CCD shift registers in order to add, shift and output signals which have been output from adjacent elements of said first and

second element array, and, in a high-resolution mode, only two types of the transfer pulses having different phases to said first and second CCD shift registers so as to shift and output signals, which have been output from said first and second pixel arrays, without addition.

Claims 13-16 (Canceled)

17. (Previously Presented) The apparatus according to claim 12, further comprising:

a light source for irradiating an original with light or making light pass through the original; and

imaging means for forming light reflected by the original into an image on said first and second element arrays.

18. (Previously Presented) The apparatus according to claim 17, further comprising:

analog gain control means for controlling an analog gain of a signal output from said first and second element arrays; and

an analog/digital converter for digitizing the signal controlled by said analog gain control means.

19. (Original) The apparatus according to claim 18, further comprising shading correction means for performing shading correction for the digitized signal.

Claims 20-21. (Canceled)

22. (Currently Amended) A processing method for an image processing apparatus including a first element array having a plurality of photoelectric conversion elements arranged in a line, a second element array shifted from the first element array by a predetermined distance in a main scanning direction and having a plurality of photoelectric conversion elements arranged in a line, a first CCD shift register, and a second CCD shift register, comprising steps of:

transferring image signals from said first element array to said first CCD shift register and from said second element array to said second CCD shift register, in parallel;

serially transferring the image signals in said first and second CCD shift registers, in a low resolution mode, in accordance with three types of transfer pulses having different phases so as to add up two signals outputted from two adjacent elements during serially transferring the signals; and

serially transferring the image signals in said first and second CCD shift registers, in a high-resolution mode, in accordance with only two types of transfer pulses having different phases so as to output signals from said first and second pixel arrays without addition.

23. (Previously Presented) The apparatus according to claim 12, wherein at least one type of the transfer pulses supplied by said pulse supply unit in the low resolution mode has a frequency which is twice as high as that of the transfer pulses supplied in the high resolution mode.

24. (Previously Presented) The apparatus according to claim 12, wherein, in the high resolution mode, said pulse supply unit alternately repeats a first operation of continuously

outputting signals from the first element array, and a second operation of continuously outputting signals from the second element array.

25. (Previously Presented) The apparatus according to claim 12, wherein, in the high resolution mode, said pulse supply unit performs a first operation that continuously outputs signals from the first element array.

26. (Currently Amended) The apparatus according to claim 12, wherein each of said first CCD shift register and said second CCD shift register have three types of register cells:

a first type of register cells that receive signals from photoelectric conversion elements and shift the received signals in response to a first pulses;

a second type of register cells positioned between two adjacent first type register cells that shift signals received from the adjacent first type of register cells in response to second or third pulses; and

a third type of register cells positioned between two adjacent first type register cells that shift signals received from the adjacent first type of register cells in accordance with the third pulses,

in the low-resolution mode, said pulse supply unit controls timing of outputting each of the first, second and third pulses so as to add up two signals outputted from two adjacent photoelectric conversion elements during serially transferring the signal in said first and second CCD shift registers, and

in the high-resolution mode, said pulse supply unit controls timing of outputting each of the first, second and third pulses so as to shift and output signals without adding two signals as is in the low-resolution mode.

27. (Currently Amended) The method according to claim 22, wherein each of said first CCD shift register and said second CCD shift register have three types of register cells:

a first type of register cells that receive signals from photoelectric conversion elements and shift the received signals in response to a first pulses;

a second type of register cells positioned between two adjacent first type register cells that shift signals received from the adjacent first type of register cells in response to second or third pulses; and

a third type of register cells positioned between two adjacent first type register cells that shift signals received from the adjacent first type of register cells in accordance with the third pulses,

in the low-resolution mode, said pulse supply unit controls timing of outputting each of the first, second and third pulses so as to add up two signals outputted from two adjacent photoelectric conversion elements during serially transferring the signal in said first and second CCD shift registers, and

in the high-resolution mode, said pulse supply unit controls timing of outputting each of the first, second and third pulses so as to shift and output signals without adding two signals as is in the low-resolution mode.